SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

STANLEY WOLF Ph.D.
Professor, Department of Electrical Engineering
California State University, Long Beach
Long Beach, California
and
Instructor, Engineering Extension, University of California, Irvine

RICHARD N. TAUBER Ph.D.
Manager of VLSI Fabrication
TRW - Microelectronics Center
Redondo Beach, California
and
Instructor, Engineering Extension, University of California, Irvine

LATTICE PRESS
Sunset Beach, California

DISCLAIMER

This publication is based on sources and information believed to be reliable, but the authors and Lattice Press disclaim any warranty or liability based on or relating to the contents of this publication.

Published by:

Lattice Press
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon and Donald Strout, Visionary Art Resources, Inc., Santa Ana, CA.

Library of Congress Cataloging in Publication Data
Wolf, Stanley and Tauber, Richard N.

Silicon Processing for the VLSI Era
Volume 1 : Process Technology

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

86-081923

ISBN 0-961672-3-7

11 12 13 14 15

PRINTED IN THE UNITED STATES OF AMERICA

Table. 4 - THERMAL PROCESSES IN VLSI FABRICATION

1. Defect Removal -
   - Thermal donor annihilation: Chap. 2
   - Formation of denuded zone on wafer surface: 2
   - Oxygen precipitate formation for intrinsic gettering: 2
   - Thermal cycle for extrinsic gettering: 2
   - Thermal reduction of oxidation-induced stacking faults: 2
   - Removal of crystal damage from ion-implantation: 2
   - Removal of radiation damage from E-gun evaporation or reactive-ion-etching: Chaps 10 & 16.
2. Active Device Fabrication -
   - Dopant incorporation by diffusion: Chap. 8
   - CVD of poly-Si, dielectrics, conductors: Chaps. 6 & 11
   - Dopant activation following ion-implantation: Chap. 9
3. Interconnect Formation -
   - Silicide formation: Chap. 11
   - Contact sintering: Chap. 10
   - CVD glass densification: Chap. 6
   - CVD glass reflow: Chap. 6

- Epitaxial deposition: Chap. 5
- Thermal Oxidation: Chap. 7
- Interface state density reduction: Chap. 7

maintain shallow junctions, controlled gate lengths, etc. Extensive research has been conducted on reducing the magnitudes of the thermal treatments to which wafers must be subjected. In this section we shall provide an overview of the role of thermal processing and describe techniques for minimizing thermal cycles. VLSI fabrication processes that entail thermal steps are first listed, although a detailed discussion is reserved for later chapters. The techniques and equipment used to perform thermal processing will be discussed, emphasizing the important topic of rapid thermal processing (RTP). Thermal treatments during VLSI fabrication can be divided according to their applications into three categories, defect removal, active device fabrication, interconnect formation. Table 4 shows the thermal cycles involved in each of these process categories.

Rapid Thermal Processing (RTP)

Many of the thermal steps in VLSI fabrication are performed at temperatures high enough (900°C) to cause unwanted dopant diffusion. Two approaches are utilized to minimize such diffusion: 1) *low-temperature processing*, such as high pressure oxidation and lower reflow temperature of CVD glasses; and 2) *short-time, high temperature processing*. Some processes are better suited to one or the other of these approaches, and thus both find useful application in VLSI fabrication. Low-temperature thermal processes are discussed in subsequent chapters.

The durations of short-time, high-temperature techniques range from seconds to a few minutes. Thus, wafers are subjected to high temperatures only long enough to achieve the desired process effect, and dopant diffusion is minimized. Short-time thermal processes, however, must be performed in specially designed systems. In conventional furnaces or reactors, the large thermal mass of the susceptors, wafer boats, and reactor walls, rules them out as possible systems for performing short thermal cycles. In addition, if large diameter wafers are heated or cooled too rapidly in a furnace, wafer warpage or slip can result.

Initial work on the rapid heating of wafers was conducted using lasers as the energy sources. Lasers allowed high heating to occur within fractions of a microsecond without significant thermal diffusion. However, the wafer surfaces had to be scanned by the small spot-size laser beams, and this caused lateral thermal gradients and resultant wafer warpage.

Subsequently, large-area incoherent energy sources were developed to overcome these limitations. These sources emit radiant light, which then heats the wafers. This allows very rapid and uniform heating and cooling. Systems are available in which such rapid thermal processing (RTP) is performed[30,31] (Fig. 18). Wafers in RTP systems are thermally isolated, so that radiant (not conductive) heating and cooling is dominant. Temperature uniformity is an important design consideration in these systems so that thermal gradients, which can cause slip or warpage, are minimized. Various heat sources are utilized, including arc lamps, tungsten-halogen lamps, and resistively-heated slotted graphite sheets. The heating chamber provides a controlled environment for the wafer, and for coupling energy from the radiant energy sources to the wafers. Most heating is done in inert atmospheres (Ar or N_2) or vacuum, although oxygen or ammonia for growth of SiO_2 and Si_3N_4 are introduced into the chamber in RTP systems.

Precise control of time and temperature is necessary to obtain reproducible RTP results. Optical pyrometers and closed-loop temperature control mechanisms are used to ensure set-point and cycle repeatability. A wide range of temperatures is also a desirable option in RTP systems since the thermal processes that can be carried out by RTP extend from 420-1150°C. A flexible, easy-to-program machine interface is also useful to allow a variety of processes to be performed in the system. The throughput of RTP systems can be quite high. Typically 60-200 125 mm wafers can be processed per hour by a single RTP system.

RTP has been successfully implemented in many thermal fabrication processes, and new applications for the technique are still being discovered. It was first widely adopted in the VLSI production environment for annealing implantation monitors (see Chap. 9). It has also has been used to grow films of SiO_2 and Si_3N_4, to form junctions in bipolar transistors through controlled diffusion, to annihilate thermal donors[29] (see following section on *Oxygen in Silicon*), and to activate dopants after ion-implantation in both single-crystal silicon and poly-Si. In interconnect formation, RTP has found use in contact sintering (with apparent reduction of hillock formation), CVD glass reflow, and the formation of Ti, Ta, Mo, and W silicides[28].

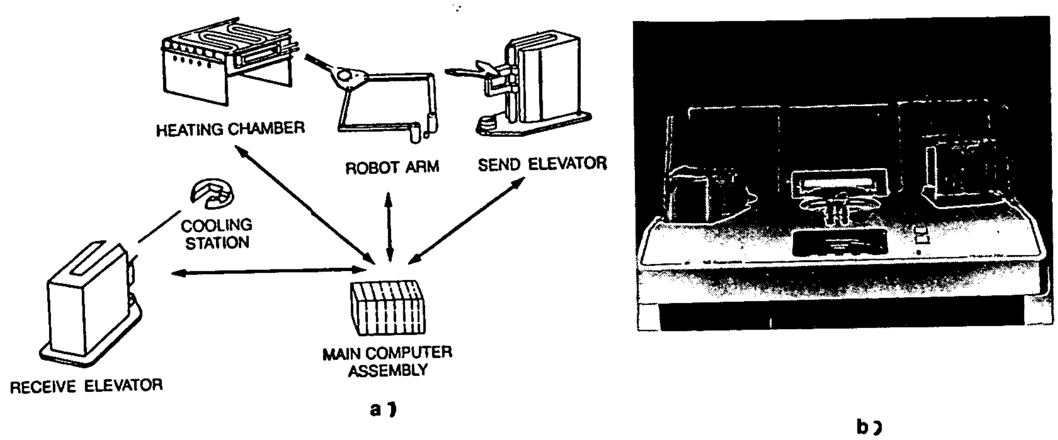

Fig. 18 (a) HEATPULSE 2106 system components. (b) Photograph of a rapid thermal processing system. Courtesy of AG Associates.